

TRANSISTOR STRUCTURE WITH THICK RECESSED SOURCE/DRAIN STRUCTURES AND FABRICATION PROCESS OF SAME

Abstract of the Disclosure

An improved transistor structure that decreases source/drain (S/D) resistance without increasing gate-to-S/D capacitance, thereby increasing device operation. S/D structures are formed into recesses formed on a semiconductor wafer through a semiconductor layer and a first layer of a buried insulator having at least two layers. A body is formed from the semiconductor layer situated between the recesses, and the body comprises a top body surface and a bottom body surface that define a body thickness. Top portions of the S/D structures are within and abut the body thickness. An improved method for forming the improved transistor structure is also described and comprises: forming recesses through a semiconductor layer and a first layer of a buried insulator so that a body is situated between the recesses; and forming S/D structures into the recesses so that top portions of the S/D structures are within and abut a body thickness.

Figures

Figure 1: A line graph showing the relationship between the number of hours spent studying and the score on a test. The x-axis represents 'Hours Studied' (0 to 10) and the y-axis represents 'Test Score' (0 to 100). The data points are as follows:

Hours Studied	Test Score
0	50
1	55
2	60
3	65
4	70
5	75
6	80
7	85
8	90
9	95
10	100

The graph shows a positive linear relationship, indicating that as the number of hours spent studying increases, the test score also increases proportionally.